What Is Claimed Is:

1. Circuitry for giving pre-emphasis to first and second differential nodes comprising:

first and second current circuits; and

switching circuitry that responds to a transition in a data signal by initially connecting both of the current circuits to only one of the nodes, and by subsequently connecting one of the current circuits only to the one of the nodes to which neither of the current circuits is initially connected if there is no further transition in the data signal for a predetermined time after the transition.

2. The circuitry defined in claim 1 wherein each of the current circuits is a current-sinking circuit.

3. The circuitry defined in claim 1 further comprising:

a power supply voltage source; and

first and second resistor circuitries respectively connecting the first and second nodes to the power supply voltage source.

4. The circuitry defined in claim 1 wherein the switching circuitry comprises:

first register circuitry for latching in and outputting the data signal shortly after the transition.

5. The circuitry defined in claim 4 wherein the switching circuitry further comprises:

second register circuitry for latching in and outputting the data signal output by the first

register circuitry shortly after the first register circuitry begins to output that data signal.

6. The circuitry defined in claim 5 wherein an output of the first register circuitry is used to determine which of the nodes the first current circuit is connected to, and wherein an output of the second register is used to determine which of the nodes the second current circuit is connected to.

7. The circuitry defined in claim 1 further comprising:

a third current circuit, and wherein the switching circuitry further responds to the transition in the data signal by initially also connecting the third current circuit to only the one of the nodes, by (during said subsequently connecting) leaving connection of the third current circuit unaltered, and by still more subsequently connecting the third current circuit only to the one of the nodes to which it is not initially connected if there is no further transition in the data signal for a further predetermined time after the transition.

8. The circuitry defined in claim 1 further comprising:

first and second output leads for respectively outputting differential signals from the first and second differential nodes.

9. The circuitry defined in claim 1 further comprising:

an output lead for outputting a single-ended output signal from only one of the first and second nodes.

10. A programmable logic device including circuitry as defined in claim 1.

11. A digital processing system comprising:

processing circuitry; and

a memory coupled to the processing circuitry, wherein at least one of the processing circuitry and the memory includes circuitry as defined in claim 1.

12. An integrated circuit including circuitry as defined in claim 1.

13. A printed circuit board on which is mounted circuitry as defined in claim 1.

14. The printed circuit board defined in claim 13 further comprising:

a memory mounted on the printed circuit board.

15. The printed circuit board defined in claim 13 further comprising:

processing circuitry mounted on the printed circuit board.

16. Output driver circuitry comprising:

first and second nodes;

a plurality of current sinking circuits; and

switching circuitry that is controllable based on a signal to be output to connect, at a first time, all of the current sinking circuits to only a selected one of the nodes, and to connect, at a second subsequent time, only a subset of the current sinking

circuits to only the one of the output nodes to which that subset was not connected at the first time if there has been no change in the signal to be output from the first time to the second time.

17. The circuitry defined in claim 16 wherein the switching circuitry comprises:

delay circuitry for establishing a delay between the first and second times.

18. The circuitry defined in claim 17 wherein the delay circuitry comprises register circuitry.

19. The circuitry defined in claim 18 wherein the signal to be output has a pulse duration, and wherein the switching circuitry further comprises circuitry for clocking the register circuitry with a clock signal having a period that is approximately equal to the pulse duration.

20. The circuitry defined in claim 18 wherein the signal to be output has a pulse duration, and wherein the switching circuitry further comprises circuitry for clocking the register circuitry with a clock signal having a period that is a fraction of the pulse duration.

21. A method of giving pre-emphasis to differential signals at a pair of nodes comprising:

connecting first and second current circuits to only a selected one of the nodes in response to receipt of an input signal; and

after a time delay interval, connecting only the second of the current circuits to only the one

of the nodes to which both of the current circuits were not connected prior to the time delay interval if the input signal is unchanged during the time delay interval.

22. The method defined in claim 21 further comprising:

after the time delay interval, leaving the first current circuit connected only to the node to which both of the current circuits were connected prior to the time delay interval if the input signal is unchanged during the time delay interval.

23. The method defined in claim 21 further comprising:

connecting the first and second nodes to a power supply voltage source through respective first and second resistors.

24. The method defined in claim 21 further comprising:

clocking the input signal through a plurality of cascaded registers to produce the time delay interval.

25. The method defined in claim 21 wherein the input signal has a predetermined pulse duration, and wherein the time delay interval is approximately equal to the pulse duration.

26. The method defined in claim 21 wherein the input signal has a predetermined pulse duration, and wherein the time delay interval is a fraction of the pulse duration.